LISTING OF THE CLAIMS

1. (Original) A driving apparatus of a liquid crystal display device, comprising:

a multiplexer array for performing time-division on inputted pixel data to supply time-divided pixel data;

a digital-to-analog converter array for converting the time-divided pixel data into pixel voltage signals; and

a demultiplexer array for driving data lines in a time-division manner to supply the converted pixel voltage signals,

wherein the digital-to-analog converter array receives a plurality of pixel voltage signal levels inputted from an external source and generates the pixel voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data.

2. (Original) The driving apparatus according to claim 1, further comprising:

a shift register array for sequentially generating a sampling signal;

a latch array for sequentially latching the pixel data by designated units in response to the sampling signal to simultaneously output the latched pixel data to the first multiplexer array; and

a buffer array for buffering the pixel voltage signal to supply the buffered signal to the demultiplexer array.

3. (Original) The driving apparatus according to claim 1, wherein the first multiplexer array includes at least an N- number (N is a positive integer) of multiplexers and performs time-division on a plurality of input pixel data to supply the time-divided pixel data, the digital-to-analog converter array converts the time-divided pixel data into the pixel voltage signals, and the demultiplexer array includes at least an N-number of demultiplexers and supplies the pixel voltage signals to a plurality of data lines.

4. (Original) The driving apparatus according to claim 3, wherein the digital-to-analog converter array includes:

at least an "N+1"-number of positive and negative digital-to-analog converters for converting the time-divided pixel data into the pixel voltage signals,

wherein the positive and negative digital-to-analog converters are alternately arranged.

5. (Original) The driving apparatus according to claim 4, further comprising:

a second multiplexer array for determining a progress path of the time-divided pixel data in response to an input polarity control signal to make the time-divided pixel data inputted to at least an N-number of positive and negative digital-to-analog converters among at least the N-number of positive and negative digital-to-analog converters; and

a third multiplexer array for determining a progress path of the pixel voltage signal in response to the polarity control signal to make the pixel voltage signal inputted to the demultiplexer array.

6. (Original) The driving apparatus according to claim 5, wherein the second multiplexer array includes at least an "N-1"-number of second multiplexers for selecting any one among outputs of at least two of the first multiplexers, the third multiplexer array includes at least an N-number of third multiplexers for selecting any one among outputs of at least two of the digital-to-analog converters, and an output of each of the first multiplexers is commonly inputted to at least the two of the second multiplexers, and an output of each of the digital-to-analog converters is commonly inputted to at least the two of the third multiplexers.

7. (Original) The driving apparatus according to claim 3, wherein the N-number of the first multiplexers include an odd-numbered multiplexer performs time-division on odd-numbered pixel data in response to an inputted first selection control signal to output the time-divided data, and an even-numbered multiplexer performs time-division on even-numbered pixel data in response to an inputted second selection control signal to output the time-divided data.

8. (Original) The driving apparatus according to claim 7, wherein the N-number of the demultiplexers include an odd-numbered demultiplexer performs time-division on odd-numbered data lines in response to the first selection control signal to drive the time-divided data lines, and an even-numbered demultiplexer performs time-division on even-numbered data lines in response to the second selection control signal to drive the time-divided data lines.

9. (Original) The driving apparatus according to claim 8, wherein the first and second selection control signals have a logical state opposite to each other, and the logical state is inverted at least for each half horizontal period.

10. (Original) The driving apparatus according to claim 9, wherein the digital-to-analog converter array generates the pixel voltage signal in use of the pixel voltage signal level having a voltage at least one step higher in absolute value than the original pixel voltage signal level in correspondence to the pixel data outputted during the first half of one horizontal period, and generates the pixel voltage signal in use of the original pixel voltage signal level in correspondence to the pixel data outputted during the second half of the one horizontal period.

11. (Original) The driving apparatus according to claim 8, wherein the first and second selection control signals have a logical state opposite to each other, and the logical state is inverted at least for each quarter horizontal period.

12. (Original) The driving apparatus according to claim 11, wherein the digital-to-analog converter array generates the pixel voltage signal in use of the pixel voltage signal level having a voltage at least one step higher in absolute value than the original pixel voltage signal level in correspondence to the pixel data outputted during the first and third quarters of one horizontal period, and generates the pixel voltage signal in use of the original pixel voltage signal level in correspondence to the pixel data outputted during the second and fourth quarters of the one horizontal period.

13. (Original) A method for driving a liquid crystal display device, comprising the steps of:

performing time-division on pixel data inputted from an external source to output time-divided pixel data;

converting the time-divided pixel data into pixel voltage signals; and

performing time-division on data lines to supply the converted pixel voltage signals thereto,

wherein the step of converting the pixel data into the pixel voltage signals includes:

generating the pixel voltage signals using a pixel voltage signal level having a voltage at least one step higher in absolute value than an original pixel voltage signal level in correspondence to at least one pixel data.

14. (Original) The method according to claim 13, wherein one horizontal period is divided into two half horizontal periods and the pixel data are time-divided to be supplied.

15. (Original) The method according to claim 14, wherein the pixel voltage signals are generated using the pixel voltage signal level having a voltage at least one step higher in absolute value than the original pixel voltage signal level in correspondence to the pixel data outputted during the first half of the one horizontal period, and is generated in use of the original pixel voltage signal level in correspondence to the pixel data outputted during the second half of the one horizontal period.

16. (Original) The method according to claim 13, wherein one horizontal period is divided into four quarter horizontal periods and the pixel data are time-divided to be supplied.

17. (Original) The method according to claim 16, wherein the pixel voltage signals are generated using the pixel voltage signal level having a voltage at least one step higher in absolute value than the original pixel voltage signal level in correspondence to the pixel data outputted during the first and third quarters of the one horizontal period, and is generated in use of the original pixel voltage signal level in correspondence to the pixel data outputted during the second and fourth quarters of the one horizontal period.